IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
Till Schlösser et al.

Serial No.: 10/720,730

Confirmation No.: 2757

Filed: November 24, 2003

For: DRAM CELL ARRANGEMENT WITH VERTICAL MOS TRANSISTORS, AND METHOD FOR ITS FABRICATION

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Group Art Unit: 2825

Examiner: Calvin Lee

Customer No.: 046798

CERTIFICATE OF MAILING
37 CFR 1.8
I hereby certify that this correspondence is being deposited on June 24, 2005, with the United States Postal Service as First Class Mail in an envelope addressed to:, Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.

June 24, 2005
Date

Gero G. McClellan

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

SUBMISSION OF FORMAL DRAWINGS

Attached please find three (3) sheets of formal drawings, with gummed labels identifying the application for which they are submitted. The Examiner is requested to substitute these formal drawings for the informal drawings used during the prosecution of the subject patent application.

Any comparison fee should be charged to Deposit Account No. 20-0782/INFN/WB0037/GGM. If any additional informalities are identified by the Examiner, please contact the undersigned attorney at (713) 623-4844.

Respectfully submitted,

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